Standards Based Networking Cores

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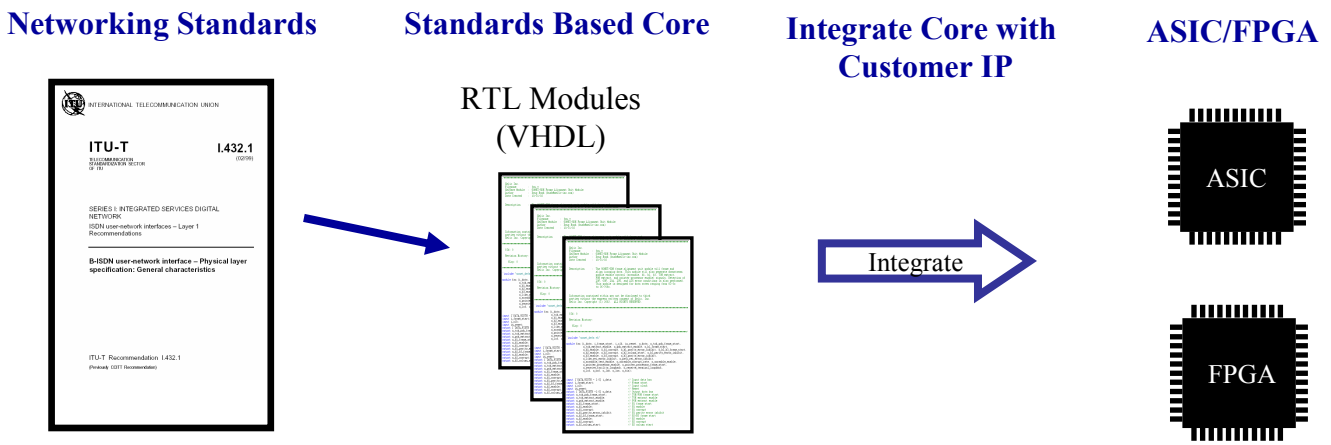
Agenda

- What are Standards Based Cores?
- Advantages
- Offerings
- Deliverables
- Support
- Validation
- Licensing Terms
- Applications
- Summary

What are Standards Based Cores?

- Xelic Standards Based Cores are Intellectual Property (IP) supporting existing and emerging networking technologies
- RTL code is developed based on functionality defined in Networking Standards to create a core that can be integrated with customer proprietary IP for ASIC and/or FGPA implementations



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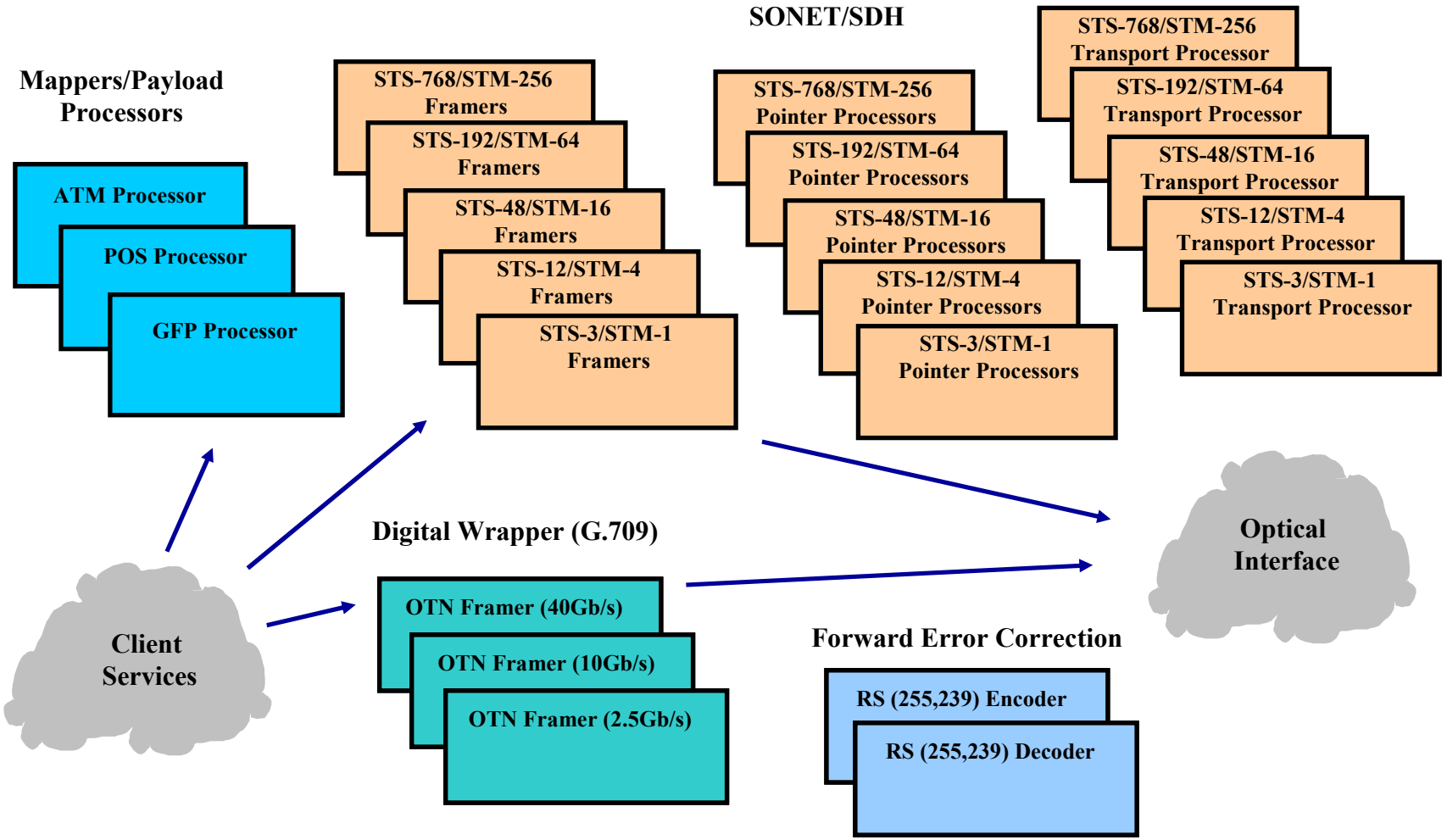
Core Advantages

- Supports standards protocols
- Accelerates proprietary IP development
- Flexible architecture
- Optimized for minimal resource utilization
- Verified and proven operation
- Fully documented
- Built in test features for debug and evaluation
- Developed using proven Xelic methodology

Core Offerings



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Core Offerings

- **SONET/SDH Cores**
  - Transport Processors (OC-3 to OC-768)
  - Path Overhead/Pointer Processors (OC-3 to OC-768) for Channelized and/or Concatenated Applications
  - Framers with Concatenated and/or Channelized Pointer Processing (STS3 to STS768)
- **Digital Wrapper (G.709) Cores**
  - Framers with FEC (2.5Gb/s to 40Gb/s)
- **Forward Error Correction Cores**
  - Reed Solomon (255, 239) Encoder
  - Reed Solomon (255, 239) Decoder
- **Mappers/Payload Processors**
  - GFP Processor
  - ATM Processor
  - POS Processor

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Core Deliverables

- Datasheet and Verification Plan
- Verification environment including self checking tests with functional models, data generators, and checkers
- Core database with netlist and/or RTL source code
- Constraints and Synthesis reports
- Fact Sheet with core resource utilization statistics
- FPGA validated cores

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Core Support

- Core customization and product integration
- Feature enhancements
- System verification support including specification, environment and test development
- Target process mapping support available including synthesis and timing closure activities
- System validation
- Product firmware and/or hardware development
- Maintenance Agreement

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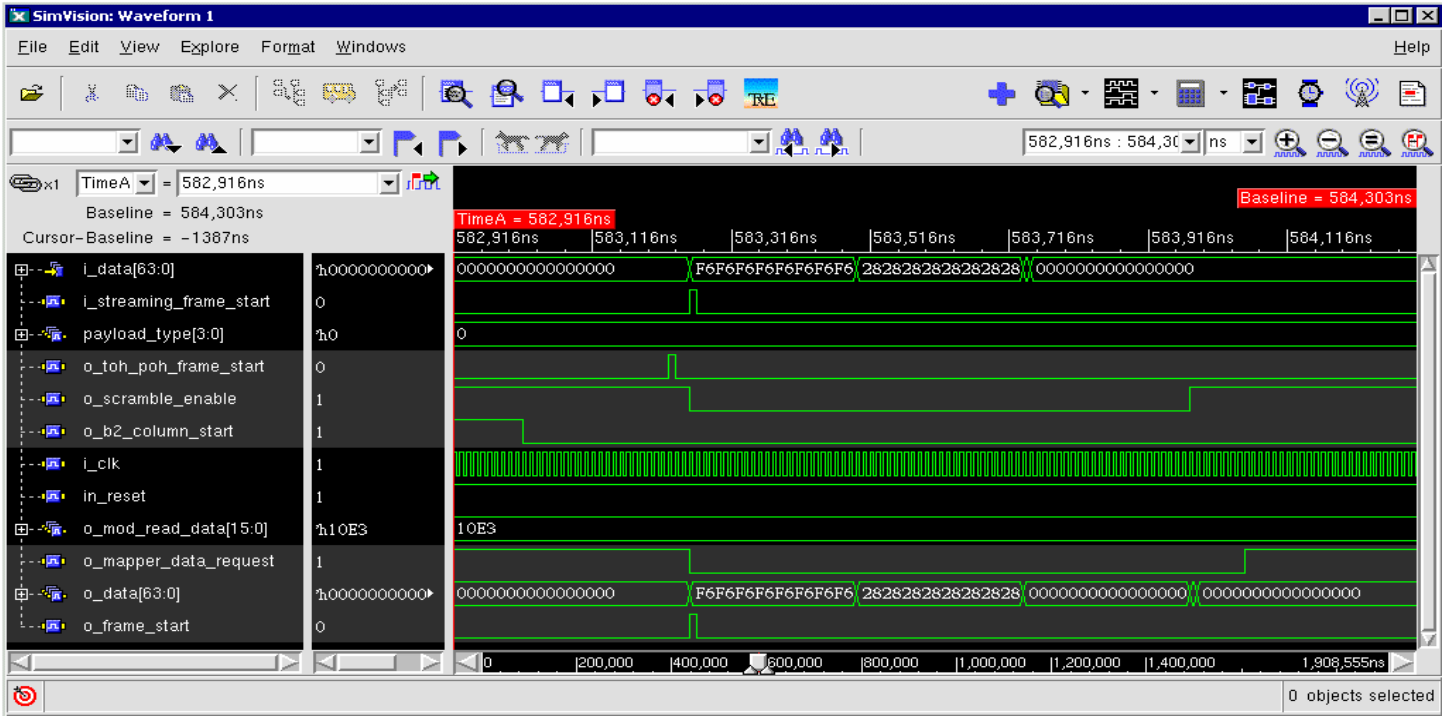
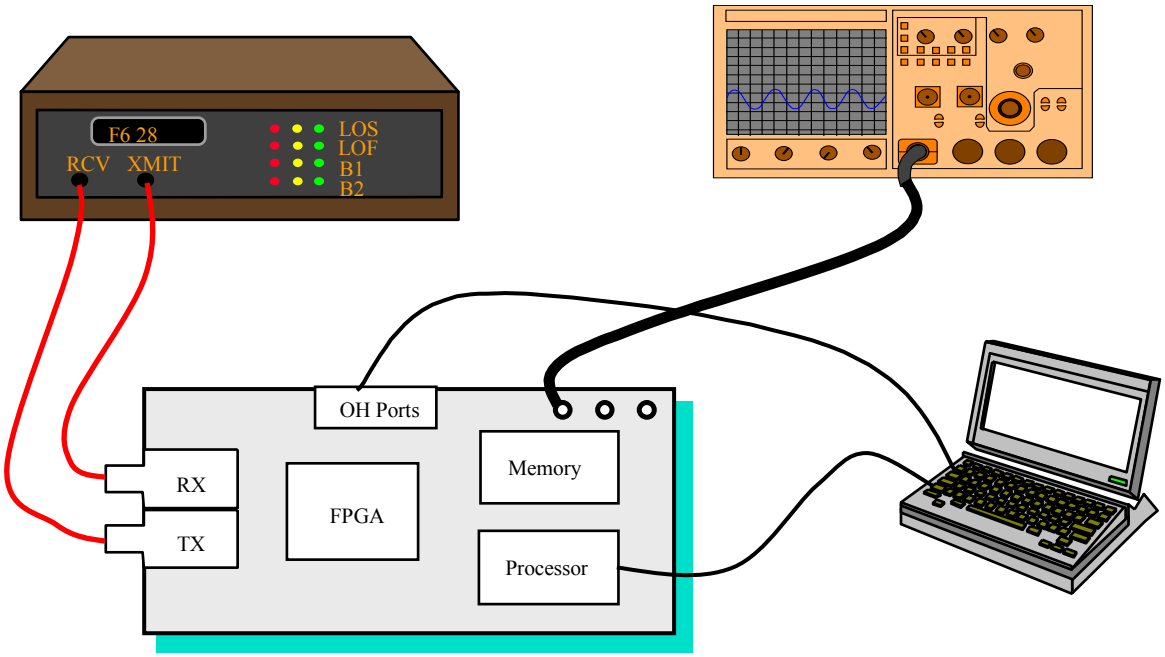
Core Validation

- Simulations verify functionality as per Verification Plan
- Xelic Verification Environment (XVE) utilized



Core Validation

- Core validation through FPGA evaluation platform and/or customer system integration



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Licensing Terms

- Flexible licensing terms
- Single use or perpetual licensing options
- Terms available for RTL and/or netlist deliverables

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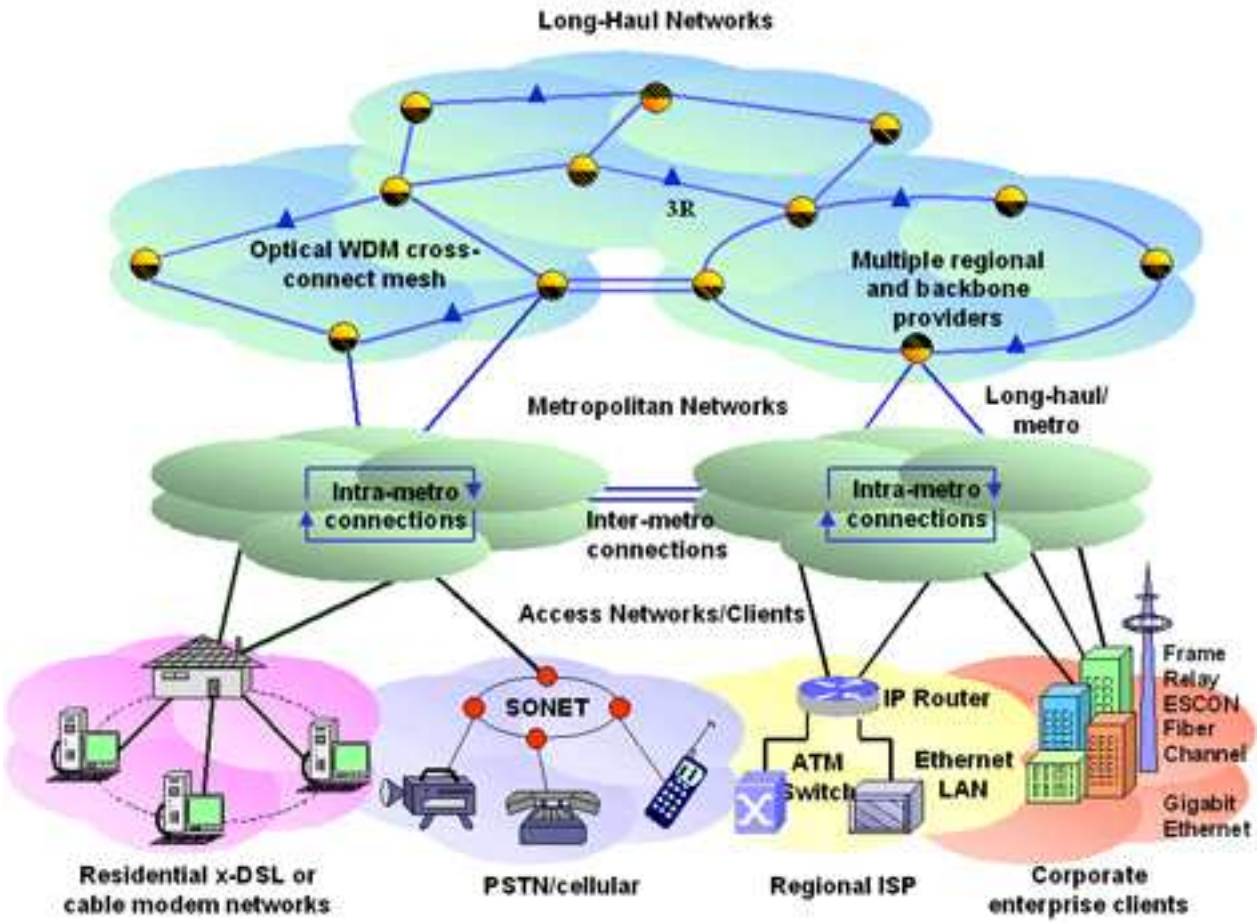
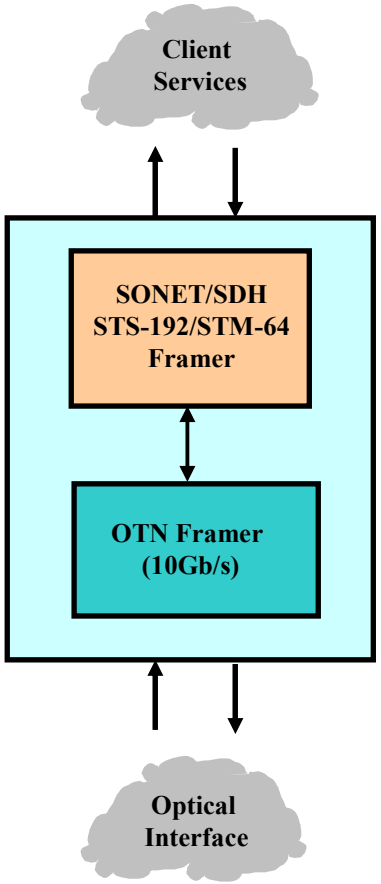
Core Applications

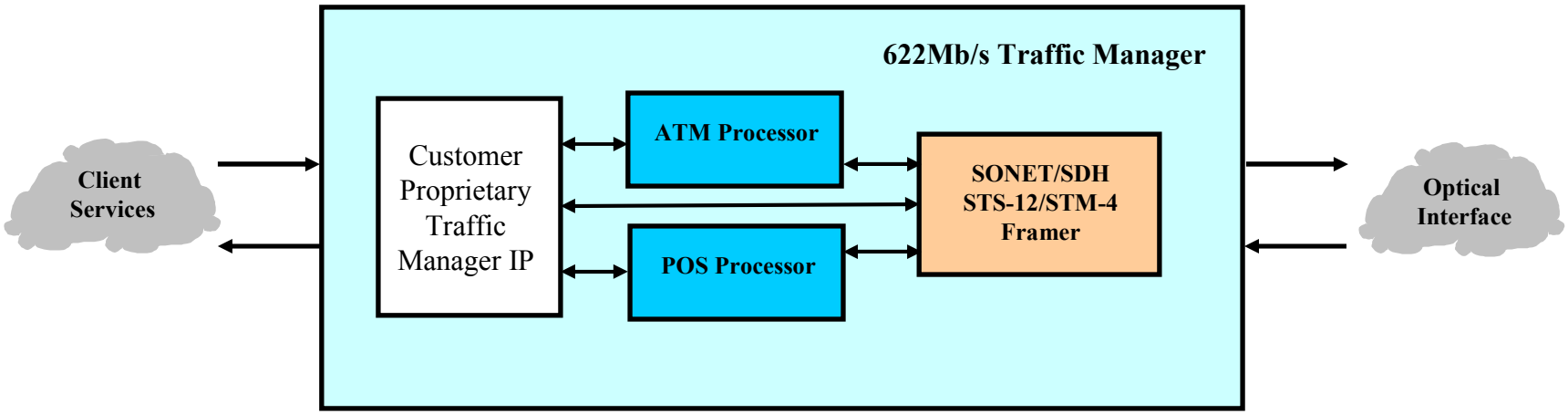


OTN - SONET/SDH Line Card Application



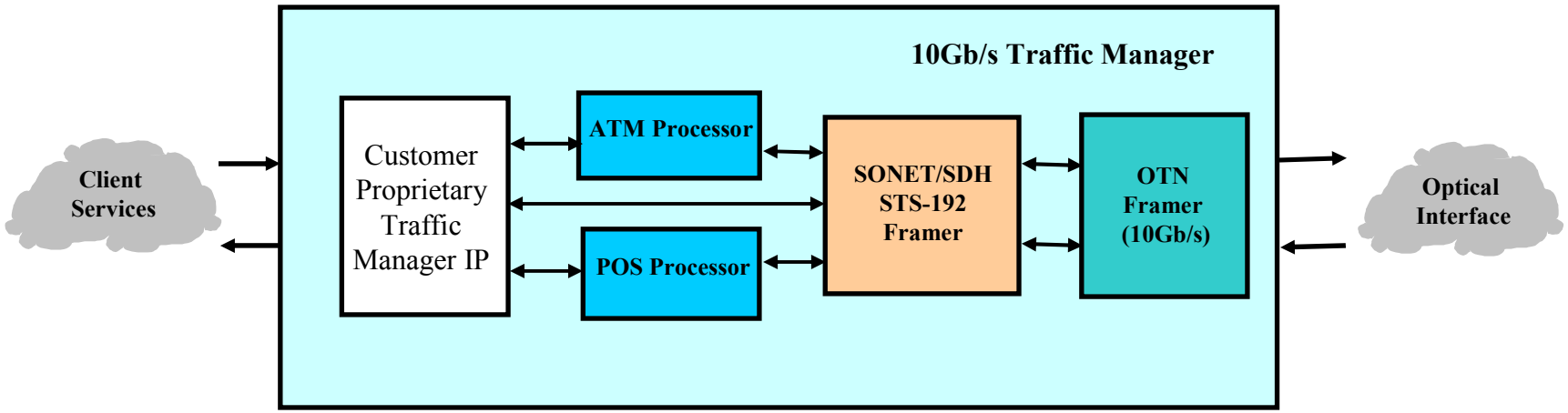
- Independent SONET and OTN overhead insertion and extraction capability
- Common processor interface
- Various error counters and error detection algorithms for system condition reporting
- Standard FEC (255, 239) OTN implementation
- Compliant with GR-253-CORE, G.709, G.798, G.707, and ANSI T1.105 standards

Traffic Manager Application (622Mb/s)



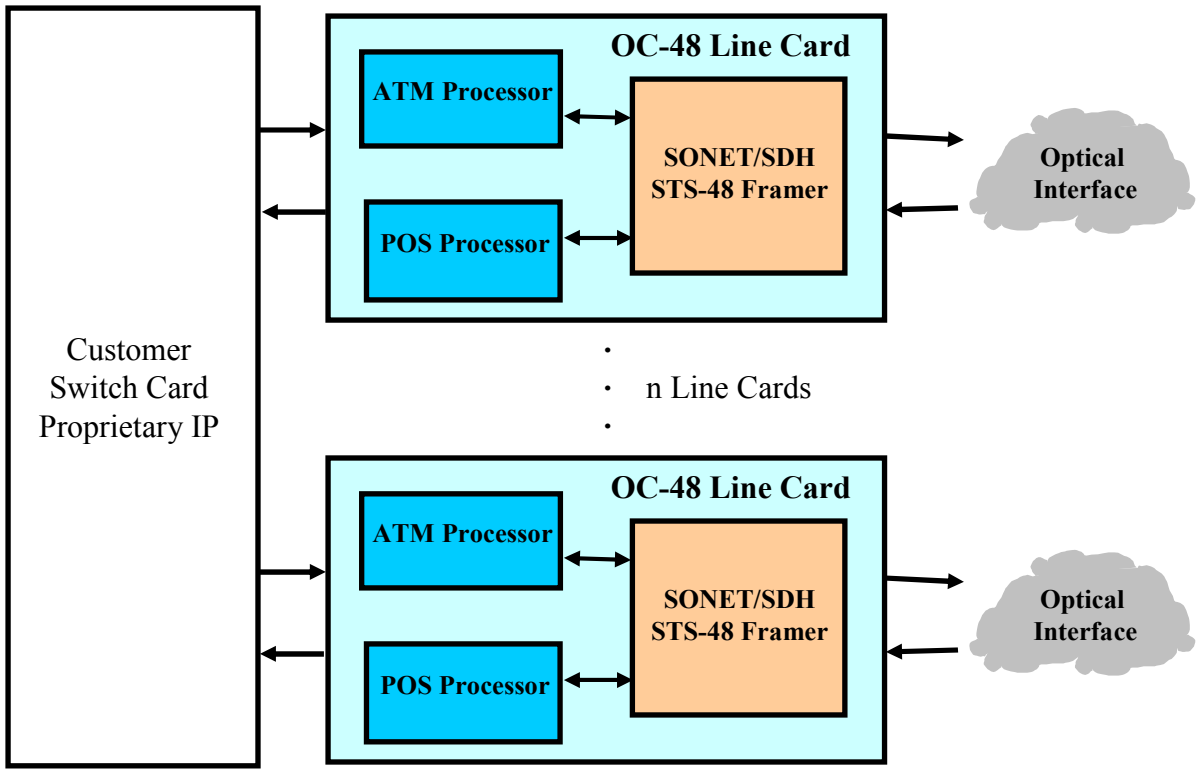
- Custom solution integrates standards based cores with customer proprietary IP
- Flexible core interfaces provide for easy integration with customer IP

Traffic Manager Application (10Gb/s)



- Proven standards based cores allow customers to focus internal resources on the development of proprietary IP
- Xelic Verification Environment can be enhanced to include customer IP with cores for validation

Switch Application



- Line Cards contain cores with processor and OH port interfaces
- Cores compliant with ATM, POS, and SONET/SDH standards
- Line Cards interface with customer switch card containing proprietary IP

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Summary

- Xelic cores provide proven solutions and allow customers to concentrate on proprietary IP development
- Standards based cores are suitable for ASIC and/or FPGA applications
- Validated FPGA functionality
- Complete documentation
- Flexible licensing terms available