Standards Based Networking Cores
Agenda

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What are Standards Based Cores?

- Xelic Standards Based Cores are Intellectual Property (IP) supporting existing and emerging networking technologies.
- RTL code is developed based on functionality defined in Networking Standards to create a core that can be integrated with customer proprietary IP for ASIC and/or FPGA implementations.
Core Advantages

• Supports standards protocols
• Accelerates proprietary IP development
• Flexible architecture
• Optimized for minimal resource utilization
• Verified and proven operation
• Fully documented
• Built in test features for debug and evaluation
• Developed using proven Xelic methodology
Core Offerings

Client Services

Mappers/Payload Processors
- ATM Processor
- POS Processor
- GFP Processor

Digital Wrapper (G.709)
- OTN Framer (40Gb/s)
- OTN Framer (10Gb/s)
- OTN Framer (2.5Gb/s)

SONET/SDH
- STS-768/STM-256 Framers
- STS-192/STM-64 Framers
- STS-48/STM-16 Framers
- STS-12/STM-4 Framers
- STS-3/STM-1 Framers

- STS-768/STM-256 Pointer Processors
- STS-192/STM-64 Pointer Processors
- STS-48/STM-16 Pointer Processors
- STS-12/STM-4 Pointer Processors
- STS-3/STM-1 Pointer Processors

Transport Processor
- STS-768/STM-256 Transport Processor
- STS-192/STM-64 Transport Processor
- STS-48/STM-16 Transport Processor
- STS-12/STM-4 Transport Processor
- STS-3/STM-1 Transport Processor

Optical Interface

Forward Error Correction
- RS (255,239) Encoder
- RS (255,239) Decoder
Core Offerings

• **SONET/SDH Cores**
  – Transport Processors (OC-3 to OC-768)
  – Path Overhead/Pointer Processors (OC-3 to OC-768)
    for Channelized and/or Concatenated Applications
  – Framers with Concatenated and/or Channelized Pointer
    Processing (STS3 to STS768)

• **Digital Wrapper (G.709) Cores**
  – Framers with FEC (2.5Gb/s to 40Gb/s)

• **Forward Error Correction Cores**
  – Reed Solomon (255, 239) Encoder
  – Reed Solomon (255, 239) Decoder

• **Mappers/Payload Processors**
  – GFP Processor
  – ATM Processor
  – POS Processor
Core Deliverables

- Datasheet and Verification Plan
- Verification environment including self checking tests with functional models, data generators, and checkers
- Core database with netlist and/or RTL source code
- Constraints and Synthesis reports
- Fact Sheet with core resource utilization statistics
- FPGA validated cores
Core Support

- Core customization and product integration
- Feature enhancements
- System verification support including specification, environment and test development
- Target process mapping support available including synthesis and timing closure activities
- System validation
- Product firmware and/or hardware development
- Maintenance Agreement
Core Validation

- Simulations verify functionality as per Verification Plan
- Xelic Verification Environment (XVE) utilized
Core Validation

• Core validation through FPGA evaluation platform and/or customer system integration
**Licensing Terms**

- Flexible licensing terms
- Single use or perpetual licensing options
- Terms available for RTL and/or netlist deliverables
Core Applications
OTN - SONET/SDH Line Card Application

- Independent SONET and OTN overhead insertion and extraction capability
- Common processor interface
- Various error counters and error detection algorithms for system condition reporting
- Standard FEC (255, 239) OTN implementation
- Compliant with GR-253-CORE, G.709, G.798, G.707, and ANSI T1.105 standards
Traffic Manager Application (622Mb/s)

- Custom solution integrates standards based cores with customer proprietary IP
- Flexible core interfaces provide for easy integration with customer IP
Traffic Manager Application (10Gb/s)

- Proven standards based cores allow customers to focus internal resources on the development of proprietary IP
- Xelic Verification Environment can be enhanced to include customer IP with cores for validation
Switch Application

- Line Cards contain cores with processor and OH port interfaces
- Cores compliant with ATM, POS, and SONET/SDH standards
- Line Cards interface with customer switch card containing proprietary IP

- OC-48 Line Card
  - ATM Processor
  - POS Processor

- SONET/SDH STS-48 Framer

- Optical Interface

- Customer Switch Card
  - Proprietary IP

- n Line Cards
Summary

- Xelic cores provide proven solutions and allow customers to concentrate on proprietary IP development
- Standards based cores are suitable for ASIC and/or FPGA applications
- Validated FPGA functionality
- Complete documentation
- Flexible licensing terms available